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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Choi et al.

Application No.: 10/798,456

Filed: March 10, 2004

Title: LINE EDGE ROUGHNESS CONTROL

Attorney Docket No.:
LAM1P187/P0930X

Examiner: Lynette T. Umez Eronini

Group: 1765

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APPEAL BRIEF TRANSMITTAL
(37 CFR 192)

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Sir:

This brief is in furtherance of the Notice of Appeal filed in this case on September 28, 2006.

This application is on behalf of

☐ Small Entity ☒ Large Entity

Pursuant to 37 CFR 1.17(f), the fee for filing the Appeal Brief is:
☐ $250.00 (Small Entity) ☒ $500.00 (Large Entity)

☐ Applicant(s) hereby petition for a _____ extension(s) of time to under 37 CFR 1.136.

If an additional extension of time is required, please consider this a petition therefor.

☐ An extension for months has already been secured and the fee paid therefor of $ is deducted from the total fee due for the total months of extension now requested.

☒ Applicant(s) believe that no (additional) Extension of Time is required; however, if it is determined that such an extension is required, Applicant(s) hereby petition that such an

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extension be granted and authorize the Commissioner to charge the required fees for an Extension of Time under 37 CFR 1.136 to Deposit Account No. 500388.

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Appeal Brief fee	$500.00
Extension Fee (if any)	$
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☐ Enclosed is Check No. in the amount of $.

☒ Charge any additional fees or credit any overpayment to Deposit Account No. 500388, (Order No. LAM1P187).

Respectfully submitted,
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December 1, 2006

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Re: Application No. 10/798,456
Attorney Docket No. LAM1P187/P1216

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Appeal Brief Transmittal (2 pg.)
Appeal Brief (20 pgs.)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex Parte Choi et al.

Application for Patent

Filed: March 10, 2004

Application No.: 10/798,456

Group Art Unit 1765

Examiner Lynette T. Umez Eronini

For:

LINE EDGE ROUGHNESS CONTROL

APPEAL BRIEF

Marc S. Hanish
Attorneys for Appellant

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1. REAL PARTY IN INTEREST

The real party in interest is the assignee, Lam Research Corporation. Address: 4650 Cushing Parkway, Fremont, CA 94536

2. RELATED APPEALS AND INTERFERENCES

It is believed that there are no other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

3. STATUS OF CLAIMS

There are a total of 24 claims pending in this application (claims 1-5, 8-15, 18-26). Claims 16-17 are withdrawn from consideration.

The claims on appeal are reproduced below in Appendix A.

4. STATUS OF AMENDMENTS

No amendment has been filed in response to the outstanding Office Action of August 24, 2006. All amendments previously filed have been entered.

5. SUMMARY OF CLAIMED SUBJECT MATTER

Summaries of independent claims 1 and 18 and dependent claims 21, 22, and 25-26 are provided herein. Summaries of dependent claims 2-5, 8-15, 19-20, and 23-

34 are not provided as these claims are not argued separately from independent claims 1 and 18.

Independent Claim 1

Claim 1 describes a method for etching an inorganic layer through a photoresist mask with an ARC layer between the layer to be etched and the photoresist mask over a substrate. This method is described at a high level on page 4, lines 1-11 and in FIGS. 1 and 3. Additionally, FIG. 2A depicts the photoresist mask and substrate. Specifically, the inorganic layer is depicted as reference number 204. The photoresist mask is depicted as reference number 220 and its ARC layer as reference number 216. The inorganic layer 204 is depicted as over a substrate 208.

The method includes placing the substrate into a processing chamber. This is described on page 4, line 16 as well as in FIG. 3, reference number 304.

The method also includes providing an ARC open gas mixture into the processing chamber. This is described on page 4, lines 17-18 and FIG. 3, reference number 308.

The ARC open gas mixture may comprise an enchant gas and a polymerization gas comprising CO and CH_3F. This is described on page 2, lines 1-2.

The method also includes forming an ARC open plasma from the ARC open gas mixture. This is depicted in FIG. 3, reference number 324.

The method also includes etching the ARC layer with the ARC open plasma until the ARC layer is opened. This is depicted in FIG. 3, reference number 328.

The method also includes stopping the ARC open gas mixture before the layer to be etched is completely etched. This is depicted in FIG. 3, reference number 332.

The method also includes etching the inorganic layer. This is described on page 4.

Independent Claim 18

Claim 18 describes a method for forming a semiconductor device. This method includes placing an inorganic dielectric layer to be etched over a substrate. This is depicted in FIG. 2A, wherein the inorganic dielectric layer to be etched, reference number 204, is placed over a substrate 208.

The method also includes forming an organic ARC layer over the layer to be etched. This is depicted in FIG. 2A, wherein the organic ARC layer 216 is formed over the inorganic dielectric layer 204.

The method also includes forming a photoresist mask over the ARC layer. This is depicted in FIG. 2A, wherein the photoresist mask 220 is formed over the ARC layer 216.

The method also includes placing the substrate into a processing chamber. This is described on page 4, line 16 as well as in FIG. 3, reference number 304.

The method also includes providing an ARC open gas mixture into the processing chamber. This is described on page 4, lines 17-18 and FIG. 3, reference number 308.

The ARC open gas mixture may comprise an enchant gas and a polymerization gas comprising CO and CH_3F. This is described on page 2, lines 1-2.

The method also includes forming an ARC open plasma from the ARC open gas mixture. This is depicted in FIG. 3, reference number 324.

The method also includes etching the ARC layer with the ARC open plasma until the ARC layer is opened. This is depicted in FIG. 3, reference number 328.

The method also includes stopping the ARC open gas mixture, so that none of the layer to be etched is etched by the ARC open plasma. This is partially depicted in

FIG. 3, reference number 332, but the added limitation that none of the layer to be etched is etched by the ARC open plasma is described on page 2, lines 13-15.

The method also includes providing an etch plasma different than the ARC open plasma. This is described on page 2, line 15.

The method also includes etching the inorganic layer to the etched with the etch plasma. This is described on page 4 and on page 2, line 16.

Dependent Claim 21

Dependent Claim 21 recites that the substrate sits atop a lower electrode providing power of 0-1000 Watts at 27 MHz and 100-1000 Watts at 2 MHz. This is described on page 5, lines 21-26 and on page 10, table 1.

Dependent Claim 22

Dependent Claim 22 recites that the temperature within the chamber is between -20 degrees and 40 degrees C. This is described on page 7, lines 30-31.

Dependent Claim 25

Dependent Claim 25 recites that the method also includes setting the pressure within the processing chamber at between 200 and 300 mTorr. This is described on page 10, table 1.

Dependent Claim 26

Dependent Claim 26 recites that the method also includes setting the pressure within the processing chamber at between 200 and 300 mTorr. This is described on page 10, table 1.

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. The rejection of claims 1, 2, 4-7, 13, 14 and 18-20 under 35 U.S.C. 103(a) as being anticipated by Naeem et al. (U.S. Patent No. 5,846,884) in view of Hineman et al., (U.S. Patent No. 6,379,872).

B. The rejection of claims 3 and 12 under 35 U.S.C. 103(a) as being unpatentable over Naeem et al. (U.S. Patent No. 5,846,884) in view of Hineman et al., (U.S. Patent No. 6,379,872) and further in view of Chen et al. (U.S. Patent No. 6,080,662).

C. The rejection of claims 8 and 10 under 35 U.S.C. 103(a) as being unpatentable over Naeem et al. (U.S. Patent No. 5,846,884) in view of Hineman et al., (U.S. Patent No. 6,379,872) and further in view of Angelopoulos et al. (U.S. Patent No. 6,316,167).

D. The rejection of claims 21, 22, 25 and 26 under 35 U.S.C. 103(a) as being unpatentable over Naeem et al. (U.S. Patent No. 5,846,884) in view of Hineman et al., (U.S. Patent No. 6,379,872) as applied to claims 1, 2, 4-7, 13, 14 and 18-20 and further in view of Hills et al. (U.S. Patent No. 6,217,786).

E. The rejection of claim 15.

7. ARGUMENT

A. The rejection of claims 1, 2, 4-7, 13, 14 and 18-20 under 35 U.S.C. 103(a) as being anticipated by Naeem et al. (U.S. Patent No. 5,846,884) in view of Hineman et al., (U.S. Patent No. 6,379,872)

On March 10, 2006, a first Office Action was issued by the Patent and Trademark Office rejecting claims 1, 2, 4-7, 13, 14, and 18-20 were rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Naeem et al. (US 5,846,884) in view of Hineman et al. (US 6,379,872 B1).

In response to this rejection, on June 9, 2006, the Applicant submitted an amendment with detailed arguments as to why these rejections were incorrect.

In a Final Office Action mailed August 24, 2006, the PTO indicated that "Applicant's arguments with respect to claims 1-5, 8-15, and 18-26 have been considered but are moot in view of the new ground(s) of rejection because the former prior art of record failed to address 'A method for etching --an inorganic dielectric -- layer . . .' as recited in (Currently Amended) Claims 1 and 18 and the limitations in (New) Claims 21-26." The body of the Final Office Action, however, fails to recite any new ground of rejection of the claims, with the exception of the rejection of the new claims 21-26. Rather, the Final Office Action merely repeats the exact same rejections using the exact same prior art, simply substituting the amended claims in for the original claims, without addressing the arguments made in the amendment or even identifying where in the (old) prior art the newly added elements can be allegedly found. The Examiner apparently simply cut and pasted the newly amended claims into the old rejection without seriously considering the arguments.

Applicant respectfully points out that such actions do not constitute a new ground of rejection. Furthermore, Applicant respectfully submits that the arguments made in the amendment are not moot. The arguments address why the cited prior art does not teach or suggest various elements of the claims. Since the Patent Office utilizes the same prior art in the Final Office Action as in the First Office Action, the arguments obviously apply equally in both.

M.P.E.P. 707(f) states "[w]here the applicant traverses any rejection, the examiner should, if he or she repeats the rejection, take note of the applicant's

argument and anwser the substance of it." Here, the Examiner has failed to follow this section of the M.P.E.P. and simply ignored the arguments made with respect to the patentability of claims 1, 2, 4-7, 13, 14, and 18-20 over Naeem and Hineman.

Specifically, neither Naeem nor Hineman nor their combination teach or suggest "a method for etching an inorganic dielectric layer" or "etching the inorganic dielectric layer" as stated in claim 1 as amended or "placing an inorganic dielectric layer to be etched over a substrate" or "etching the inorganic dielectric layer to be etched with the etch plasma" as stated in claim 18 as amended. Particularly, Naemm describes altering the sputter in the etch from a high sputter to a low sputter prior to the metallization layer being penetrated. Col. 7, lines 4-20. Naemm's concern is the prevention of a high sputter during etching of the metallization layer. Essentially, Naemm wishes to protect the metallization layer from the etch that penetrates the ARC layer. Naemm does not teach or suggest trying to protect an inorganic dielectric layer during the etch that penetrates the ARC layer, or any other etch for that matter, despite Naemm clearly teaching a dielectric layer (see FIG. 1B). The presently claimed invention, on the other hand, describes a method for etching an inorganic dielectric layer, which is a process that does not occur in Naemm until long after the inventive process in Naemm is completed. The presently claimed invention acts to protect the dielectric layer, which as described above Naemm is indifferent about.

Hineman teaches halting a first plasma etch process prior to completion of the ARC etch. Hineman accomplishes this, however, by using a pre-selected duration or through the use of a detector that detects when etching of the layer beneath the ARC occurs (see Col. 3, line 56 through Col. 4, line 7). Hineman does not attempt to utilize specialized gases, pressures, or other chamber settings to help reduce or eliminate the erosion of the substrate during the first plasma etch. As such, Applicant respectfully submits that claims 1 and 18 are in condition for allowance.

As to dependent claims 2, 4-7, 13, 14, and 19-20, these claims are also patentably distinct from the cited references for at least the same reasons as those recited above for the independent claims, upon which they ultimately depend. These dependent claims recite additional limitations that further distinguish these dependent claims from the cited references.

Since the PTO has failed to address these arguments in the Final Office Action, Applicant is unable to determine whether they have actually been considered. In light of the same prior art being used to reject the same claims, it seems clear that these arguments are relevant to the rejections in the Final Office Action and should have been addressed in the Final Office Action.

B. The rejection of claims 3 and 12 under 35 U.S.C. 103(a) as being unpatentable over Naeem et al. (U.S. Patent No. 5,846,884) in view of Hineman et al., (U.S. Patent No. 6,379,872) and further in view of Chen et al. (U.S. Patent No. 6,080,662)

The Examiner rejected claims 3 and 12 under 35 U.S.C. 103(a) as being allegedly unpatentable over Naem in view of Hineman, and further in view of Chen et al. (US 6,080,662). Specifically, the Examiner argues that Chen discloses an etching process that uses 0-200 sccm of CO and that it would be obvious to incorporate Chen into Naem and Hineman.

Claims 3 and 12 are not argued separately from parent claim 1. As such, Applicant herein incorporates by reference the argument above relating to rejection of claims 1, 2, 4-7, 13, 14 and 18-20.

C. The rejection of claims 8 and 10 under 35 U.S.C. 103(a) as being unpatentable over Naeem et al. (U.S. Patent No. 5,846,884) in view of Hineman et al., (U.S. Patent No. 6,379,872) and further in view of Angelopoulos et al. (U.S. Patent No. 6,316,167)

The Examiner rejected claims 8 and 10 under 35 U.S.C. 103(a) as being allegedly unpatentable over Naem in view of Hineman, and further in view of Angelopoulos et al. (US 6,316,167). Specifically, the Examiner argues that Angelopoulos discloses an organic ARC layer and a photoresist mask of 193 or higher generation and that it would be obvious to incorporate Angelopoulos into Naem and Hineman.

Claims 8 and 10 are not argued separately from parent claim 1. As such, Applicant herein incorporates by reference the argument above relating to rejection of claims 1, 2, 4-7, 13, 14 and 18-20.

D. The rejection of claims 21, 22, 25 and 26 under 35 U.S.C. 103(a) as being unpatentable over Naeem et al. (U.S. Patent No. 5,846,884) in view of Hineman et al., (U.S. Patent No. 6,379,872) as applied to claims 1, 2, 4-7, 13, 14 and 18-20 and further in view of Hills et al. (U.S. Patent No. 6,217,786)

The Examiner rejected claims 21, 22, 25, and 26 under 35 U.S.C. 103(a) as being allegedly unpatentable over Naeem in view of Hineman and further in view of Hills. Specifically, the Examiner points to table 1 in Col. 6 of Hills as allegedly teaching various processing parameters of claims 21, 22, 25, and 26.

Claim 21

Claim 21 indicates that the substrate sits atop a lower electrode providing power of 0-1000 Watts at 27 MHz and 100-1000 Watts at 2 MHz. Contrary to what is stated in the Final Office Action, however, Hills fails to teach a lower electrode providing 0-1000 Watts at 27 Mhz. Table 1 of Hills indicates a top electrode frequency of 13-40 MHz and a bottom electrode frequency of 1-4 MHz. Hills fails to teach operating the bottom electrode at any frequency other than 1-4 MHz. None of the references, therefore, teach or suggest a lower electrode providing power of 0-1000 Watts at 27 MHz. As such, Applicant respectfully submits that claim 21 is in condition for allowance.

Claim 22

Claim 22 indicates that the temperature within the chamber is between -20 degree and 40 degrees C. While Hills teaches temperatures within that range for etching of an inorganic dielectric layer, but does not teach anything about doing so during the etching of the ARC layer. The etching of the inorganic layer is merely the final step of claim 1, from which claim 22 ultimately depends. The wording of claim 22 implies that the temperature is kept within the desired range for each of the steps performed in claim 1, not just the final step. While it may be obvious to etch an

inorganic dielectric layer at the specified temperatures, it is not obvious to perform the other steps of claim 1 at those temperatures.

The indicated temperature range aids in the prevention of accidental etching of the inorganic dielectric layer during the etching of the ARC layer in case the ARC etch is not stopped in time. None of the cited references contain such safety precautions if the ARC etch is not stopped in time and thus their combination would also suffer from such a significant drawback and/or it would not be obvious to combine these references in the first place. As such, Applicant respectfully submits that claim 22 is in condition for allowance.

Claims 25-26

As to claims 25-26, a specific chamber pressure range (200 to 300 mTorr) is provided. In Naeem, there are several layers between the ARC layer and the substrate, specifically, referring to FIG. 1, a bottom barrier 104, a metallization layer 106, a first top barrier 108, and a second top barrier 110. The problem in Naemm is not damage caused to the substrate itself, but the difficulty in cleaning the sidewalls that are covered in portions of the inorganic material from the substrate and/or metallization layer. Naeem's solution is to increase the sputter when breaking through the organic ARC layer 112, essentially intentionally causing organic materials to spray on the sidewalls. By doing so, when the eventual inorganic material winds up hitting the sidewalls, it is much easier to remove (see Col. 6, lines 14-32). Notably, the pressure range for the break-through stage is provided in Table 1, and even the broadest range (2-10 mTorr) falls outside the 200 to 300 mTorr range of claims 25-26.

Hineman teaches halting a first plasma etch process prior to completion of the ARC etch. Hineman accomplishes this, however, by using a pre-selected duration or through the use of a detector that detects when etching of the layer beneath the ARC occurs (see Col. 3, line 56 through Col. 4, line 7). Hineman does not attempt to utilize specialized gases, pressures, or other chamber settings to help reduce or eliminate the erosion of the substrate during the first plasma etch. While various

pressure settings are described (Col. 5, lines 2-23), each of these pressure settings falls outside the 200 to 300 mTorr range of claims 25-26.

While Hills teaches pressures within that range for etching of an inorganic dielectric layer, it does not teach anything about doing so during the etching of the ARC layer. The etching of the inorganic layer is merely the final step of claims 1 and 18, from which claims 25 and 26 ultimately depend, respectively. The wording of claims 25 and 26 implies that the pressure is kept within the desired range for each of the steps performed in claims 1 and 18, respectively, not just the final step. While it may be obvious to etch an inorganic dielectric layer at the specified pressures, it is not obvious to perform the other steps of claims 1 and 18 at those pressures.

The indicated pressure range aids in the prevention of accidental etching of the inorganic dielectric layer during the etching of the ARC layer in case the ARC etch is not stopped in time. None of the cited references contain such safety precautions if the ARC etch is not stopped in time and thus their combination would also suffer from such a significant drawback and/or it would not be obvious to combine these references in the first place. As such, Applicant respectfully submits that claims 25-26 are in condition for allowance.

E. The rejection of claim 15

The PTO has failed to provide any basis for the rejection of claim 15. Specifically, the "Office Action Summary" of the Final Office Action lists claims 1-5, 8-15, and 18-26 as being rejected, but the body of the Final Office Action fails to recite a basis for the rejection of claim 15. This omission was pointed out by the Applicant in the Amendment of June 9, 2006 with respect to the Office Action of March 10, 2006, which was also missing the basis for the rejection of claim 15. Nevertheless, this omission was never corrected by the PTO and Applicant still is unable to determine what, if any, reasons the PTO has for the rejection of claim 15.

M.P.E.P. 707.07(d) states "[w]here a claim is refused for any reason relating to the merits thereof it should be 'rejected' and the ground of rejection fully and clearly stated, and the word 'reject' must be used. The examiner should designate the

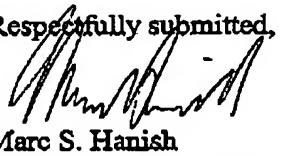
statutory basis for any ground of rejection by express reference to a section of 35 U.S.C. in the opening sentence of each round of rejection."

Here, the Examiner has violated the M.P.E.P. by failing to provide a statutory basis for the rejection of claim 15. As such, Applicant respectfully submits that claim 15 is in condition for allowance.

Conclusion

Accordingly, it is respectfully requested that the Board reverse the Examiner's rejections and remand the application to the Examiner with directions to allow all claims.

Respectfully submitted,



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8. CLAIMS APPENDIX

1. (Previously Presented) A method for etching an inorganic dielectric layer through a photoresist mask with an ARC layer between the layer to be etched and the photoresist mask over a substrate, comprising:

placing the substrate into a processing chamber;

providing an ARC open gas mixture into the processing chamber, wherein the ARC open gas mixture comprises:

an etchant gas; and

a polymerization gas comprising CO and CH_3F;

forming an ARC open plasma from the ARC open gas mixture;

etching the ARC layer with the ARC open plasma until the ARC layer is opened;

stopping the ARC open gas mixture before the layer to be etched is completely etched; and

etching the inorganic dielectric layer.

2. (Original) The method, as recited in claim 1, wherein ARC open plasma highly selectively etches the ARC with respect to the layer to be etched.

3. (Original) The method, as recited in claim 2, wherein the flow rate of CO is at least 150 sccm.

4. (Original) The method, as recited in claim 3, wherein the ARC open gas mixture further comprises an etch rate booster, wherein the etch rate booster is O_2.

5. (Original) The method, as recited in claim 4, wherein the layer to be etched is a dielectric layer and wherein the etchant gas comprises at least one of an N_2 and H_2 mixture and CF_4.

6. (Canceled)

7. (Canceled)

8. (Previously Presented) The method, as recited in claim 1, wherein the photoresist mask is of a 193 or higher generation photoresist.

9. (Original) The method, as recited in claim 8, wherein the ARC layer is of an organic material.

10. (Original) The method, as recited in claim 2, wherein the ARC layer is of an organic material and wherein the photoresist mask is of a 193 or higher generation photoresist.

11. (Original) The method, as recited in claim 1, wherein the ARC layer is of an organic material and wherein the photoresist mask is of a 193 or higher generation photoresist and wherein the ARC open plasma etches the ARC with respect to the layer to be etched with a selectivity greater than 50:1.

12. (Original) The method, as recited in claim 11, wherein the flow rate of CO is at least 150 sccm, and wherein the layer to be etched is silicon oxide.

13. (Original) The method, as recited in claim 12, wherein the ARC open gas mixture further comprises an etch rate booster, wherein the etch rate booster is O_2.

14. (Original) The method, as recited in claim 1, wherein the ARC open plasma does not etch the layer to be etched.

15. (Original) The method, as recited in claim 14, wherein the ARC layer is of an organic material and wherein the photoresist mask is of a 193 or higher generation photoresist and the layer to be etched is silicon oxide.

16. (Withdrawn) A semiconductor device formed by the method of claim 1.

17. (Withdrawn) An apparatus with computer readable media for performing the method of claim 1.

18. (Previously Presented) A method for forming a semiconductor device, comprising:

placing an inorganic dielectric layer to be etched over a substrate;

forming an organic ARC layer over the layer to be etched;

forming a photoresist mask over the ARC layer;

placing the substrate into a processing chamber;

providing an ARC open gas mixture into the processing chamber, wherein the ARC open gas mixture comprises:

an etchant gas; and

a polymerization gas comprising CO and CH_3F;

forming an ARC open plasma from the ARC open gas mixture;

etching the ARC layer with the ARC open plasma until the ARC layer is opened;

stopping the ARC open gas mixture, so that none of the layer to be etched is etched by the ARC open plasma;

providing an etch plasma different than the ARC open plasma; and

etching the inorganic dielectric layer to be etched with the etch plasma.

19. (Original) The method, as recited in claim 18, wherein the ARC open gas mixture further comprises an etch rate booster, wherein the etch rate booster is O_2.

20. (Original) The method, as recited in claim 4, wherein the layer to be etched is a dielectric layer and wherein the etch plasma is formed from an etchant gas comprising at least one of an N_2 and H_2 mixture and CF_4.

21. (Previously Presented) The method, as recited in claim 1, wherein said substrate sits atop a lower electrode providing power of 0-1000 Watts at 27 MHz and 100-1000 Watts at 2 MHz.

22. (Previously Presented) The method, as recited in claim 21, wherein the temperature within said chamber is between -20 degrees and 40 degrees C.

23. (Previously Presented) The method of claim 1, wherein the inorganic dielectric layer is silicon oxide.

24. (Previously Presented) The method of claim 18, wherein the inorganic dielectric layer is silicon oxide.

25. (Previously Presented) The method of claim 1, further comprising:

setting the pressure within said processing chamber at between 200 and 300 mTorr.

26. (Previously Presented) The method of claim 18, further comprising:

setting the pressure within said processing chamber at between 200 and 300 mTorr.

9. EVIDENCE APPENDIX

None